9725

Hardware Design

User Guide

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Preface

Welcome to the Hardware Design Guide for the 9725 Acceleration Processor. This document provides recommendations to the system designer using Hifn's 9725 processor for schematic design and PCB layout. As with most modern silicon devices, internal functions and off-chip interface operate at frequencies greater than 100MHz and their layout and routing careful attention and adherence to general and Hifn-specific high-speed design rules.

Audience

This document is intended for integrators and application developers responsible for and familiar with software and hardware architecture of a target system. Knowledge of high-speed design practices is assumed.

Prerequisite

Before proceeding, you should generally understand:

- Circuit-level hardware design
- PCB layout concepts
- General networking concepts

Document Organization

This document is organized as follows:

Related Documents

The following documents can be used as a reference to this document.

DS-0161 *9725 Data Sheet*

Customer Support

For technical support about this product, please contact your local Hifn sales office, representative, or distributor.

For general information about Hifn and Hifn products refer to: www.hifn.com

1 Power and Ground Considerations

This chapter provides detailed information about the digital and analog power supply connections on the 9725 device. Generally speaking, analog supplies can be derived from the same power source as the digital supplies, but are more noise-sensitive and require additional filtering and careful layout/routing.

1.1 PLL Power Supply

The PLL power supply on the 9725 chip should be filtered to prevent board and power supply-switching noise from entering the sensitive PLL circuits. Refer to Figure 1-1 for the components and connections for the 9725 PLL power supply interfaces.

The filter components should be places as close as possible to the associated balls on the 9725 chip, even though the PLL signals are on the inside rows of the device. The routing associated with these filter components should on a layer that is adjacent to a ground plane. No high speed digital traces should run parallel to the PLL traces. The following circuit describes the recommended bypass filter for the 9725 analog and digital power supply connections.

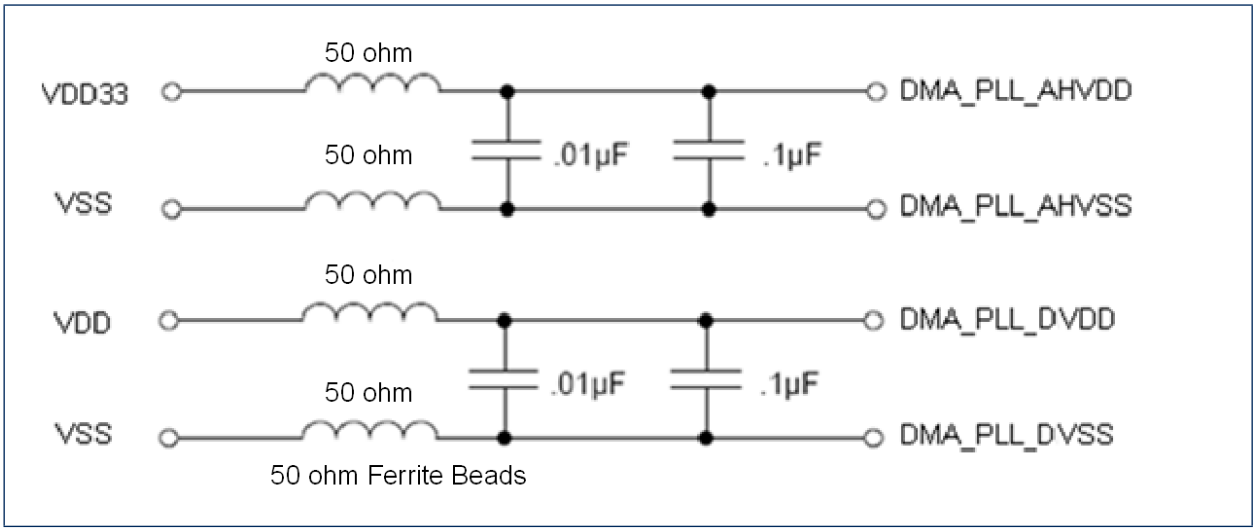

Figure 1-1. Bypass Filter for PLL Power Supplies

Care must be taken when routing the DMA_PLL_AHVSS and DMA_PLL_DVSS power traces to the ferrite beads to minimize the inductance of the traces.

The 50Ω ferrite beads should be similar to:

MFR: Murata
MFR P/N: BLM31P500SPT
Description: IND FB BLM31P500SPT 50Ω 1206

Smaller ferrite may be used (0805 for instance), but 50Ω at 100MHz is recommended.

1.2 Device Power Supply Filtering

Each power rail requires a 10µF capacitor plus several high-frequency bypass capacitors in the range of 0.001µF to 0.1µF. Table 1-1 provides guidelines for selecting the capacitance values and number of capacitors required. For both core and I/O supplies, there should be a proportioned mix of 0.001µF, 0.01µF and 0.1uF capacitors, and these capacitors should be of good quality dielectric such as X7R. The number of capacitors listed in Table 1-1 has been proven to achieve good noise and ripple margin.

Table 1-1. Suggested Number of Bypass Capacitors per Power Rail

Power Rail	10µF (3216) (Required)	0.1µF (0402), or 0.01µF (0402), or 0.001µF (0402)
VDD33	1	4
VDD18	1	1
VDD	1	15
PCIE_VDD	1	3
PCIE_VDDA	1	3
PCIE_VDDB	1	1
PCIE_VTT	1	1

Orient the capacitors close to the device as possible and adjacent to the power pads. Decoupling capacitors should be connected to the power planes with short, thick traces and vias as long, thin traces are more inductive and will reduce the intended effect of decoupling capacitors.

It is also important to have the decoupling capacitors for the core placed as close as possible to the core supply balls. This can be a challenge because space on the bottom of the device is limited. Figure 1-2 illustrates a placement of bypass capacitors on the bottom side of the PCB.

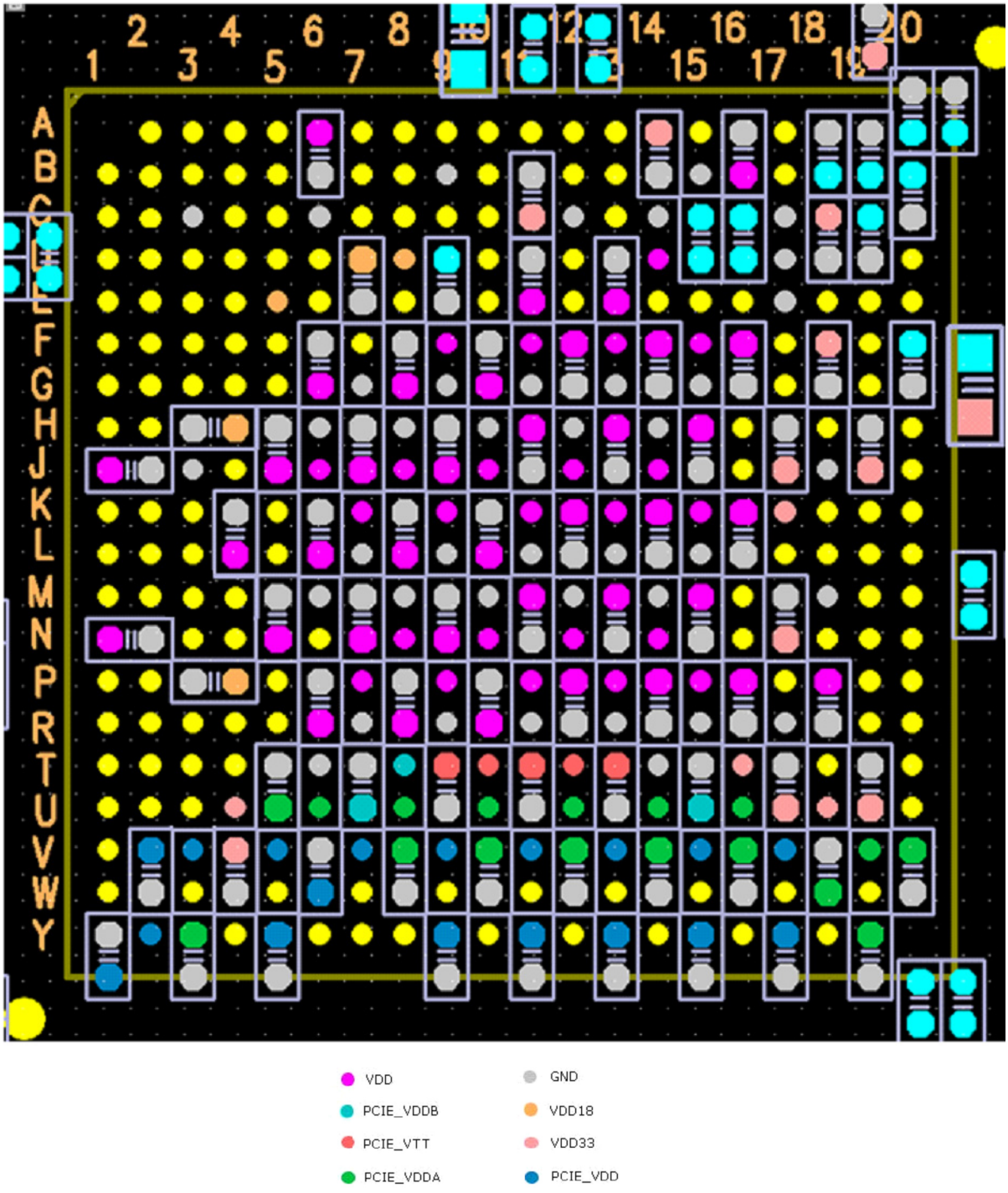

Figure 1-2. Suggested Placement of Bypass Capacitors on the Bottom Side of the PCB

1.3 Power Sequencing

The 9725 power supplies must be powered up in the sequence described in this section to ensure that the device does not latchup or have a shorted power supply condition after power-up.

For the 9725 I/O configuration, with the exception of the PCIE_VTT supply, different voltages are supplied to the core oxide and the second layer oxide, and there is the equivalent of a parasitic diode from the core power rail to the I/O power rail. Therefore, if the core is powered on before the I/O power, there will be current flowing through this parasitic diode which may damage the device or lead to a reduced operational life.

It is important not to exceed the power sequencing time limit to avoid bus conflicts. The time between power supplies power up should be between 0ms and 10ms (0ms<t<10ms), to avoid bus conflicts.

For PCIE power supplies, although PCIE_VTT is higher than PCIE_VDD, it must be powered after VDD for reliable operation.

The 9725 power supplies can be brought up simultaneously (with the exception of the PCIE_VTT) with the following constraints:

- The 1V supply can NEVER exceed the level of the 1.8V supply or the 3.3V supply.
- The 1.8V supply can NEVER exceed the level of the 3.3V supply.
- The PCIE_VTT supply must be power AFTER PCIE_VDD.

The figure below illustrates the power sequencing requirement.

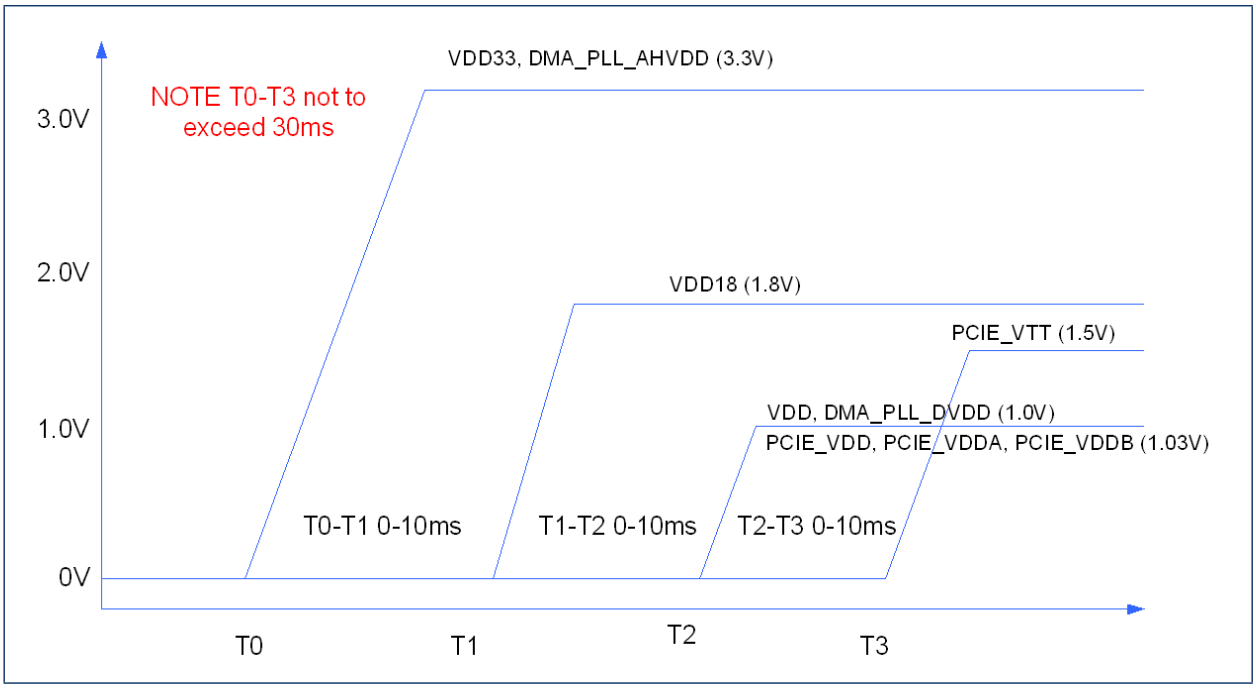

Figure 1-3. Power Supply Sequencing

The power down sequence is the opposite of the power-up sequence. Power down the lower core voltage first and the higher I/O supply second.

2 PCI Express Interface Considerations

2.1 Reference Clock AC Coupling Capacitor

The 9725 clock inputs require an AC-coupled interface. However, the LVDS driver requires a DC termination path, therefore a 2KΩ resistor should be inserted in the signal path before the AC-coupling capacitors for proper operation. This resistor can be placed anywhere along the signal path between the clock source and the AC-coupling capacitors. Note that the effective termination resistance seen by the clock source is about 95Ω due to the parallel combination of this external resistor and the 9725 internal termination resistor.

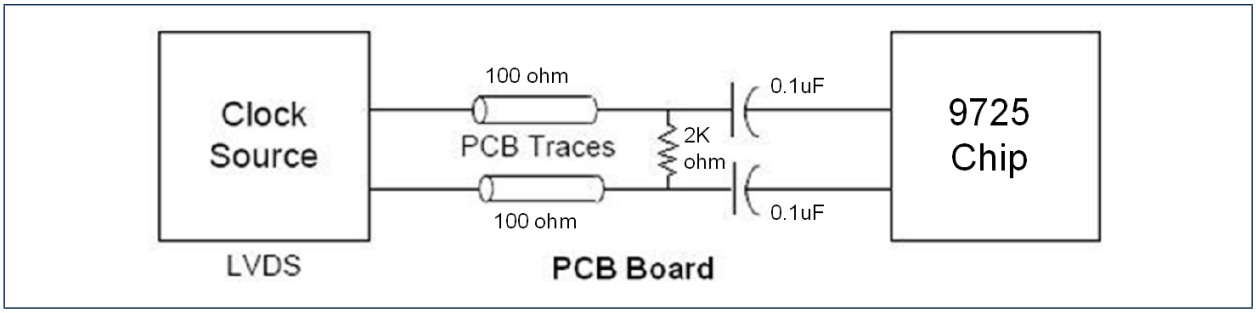

Figure 2-1. Reference Clock Decoupling Circuit

2.2 PCIe Configuration

The drive current and equalization default configuration is listed in Table 2-1.

Table 2-1. PCIe Default Configuration

Signal	Input/ Output	Type	Default Value	Description
Termination Signals				
TXTERMADJ[1:0]	Input	CMOS	00	Transmit Termination Adjust. Control bus to adjust transmit termination values. Decodes as follows: b00 = Tx termination to nominal (~50Ω) b01 = Tx termination to (nominal - 17%) b10 = Tx termination to (nominal + 10%) b11 = Tx termination to (nominal - 15%)
RXTERMADJ[1:0]	Input	CMOS	00	Receive Termination Adjust. Control bus to adjust receive termination values. Decodes as follows: b00 = Rx termination to nominal (~50Ω) b01 = Rx termination to (nominal - 17%) b10 = Rx termination to (nominal + 10%) b11 = Rx termination to (nominal - 15%)
SerDes Mode Signals				
HIDRV	Input	CMOS	0	High Drive. Used to increase the nominal value of the lane's driver current level (see Table 2-2).
LODRV	Input	CMOS	0	Low Drive. Used to decrease the nominal value of the lane's driver current level (see Table 2-2).

Table 2-1. PCIe Default Configuration

Signal	Input/ Output	Type	Default Value	Description
DTX[3:0]	Input	CMOS	0000	Driver Transmit Level. 4-bit digital word used to control the driver current level (see Table 2-3).
DEQ[3:0]	Input	CMOS	0000	Driver Equalization. 4-bit digital word used to control the driver equalization level (see Table 2-4).
RXEQCTL[1:0]	Input	CMOS	10	Receive Equalization Control. Used to select for the global receive equalizer of each lane. Decodes as follows (see Table 2-5): b00 = max. Rx Eq b01 = min. Rx Eq b10 = Rx Eq off b11 = Rx Eq off

Table 2-2. Nominal HIDRV and LODRV Current Values

HIDRV	LODRV	Nominal Driver Current
0	0	20 mA
0	1	10 mA
1	0	28 mA
1	1	Reserved

Table 2-3. DTX[3:0] Current Values

DTX[3:0]	Actual Current / Nominal Current
0000	1.00
0001	1.05
0010	1.10
0011	1.15
0100	1.20
0101	1.25
0110	1.30
0111	1.35
1000	0.60
1001	0.65
1010	0.70

Table 2-3. DTX[3:0] Current Values

DTX[3:0]	Actual Current / Nominal Current
1011	0.75
1100	0.80
1101	0.85
1110	0.90
1111	0.95

Table 2-4. DEQ[3:0] Values

DEQ[3:0]	(ITX - IEQ) / ITX	De-emphasis (dB)
0000	1.00	0.00
0001	0.96	-0.35
0010	0.92	-0.72
0011	0.88	-1.11
0100	0.84	-1.51
0101	0.80	-1.94
0110	0.76	-2.38
0111	0.72	-2.85
1000	0.68	-3.35
1001	0.64	-3.88
1010	0.60	-4.44
1011	0.56	-5.04
1100	0.52	-5.68
1101	0.48	-6.38
1110	0.44	-7.13
1111	0.40	-7.96

Table 2-5. RXEQCTL[1:0] Settings

RXEQCTL[1:0]	Rx Eq Setting	Input Jitter (Note 1)	Channel Length (Note 2)
00	Max. Rx EQ	jitter > 0.25 UI	two or more connectors > 20"
10	Min. Rx EQ	0.1 UI < jitter < 0.25 UI	up to two connectors between 8" and 20"
xx	Rx EQ off	jitter < 0.1 UI	one connector 8" or less
Notes: 1. Unit Intervals (UI) = 400ps 2. Assumes channel based on standard FR4 material.			

2.3 PCIe Signals Routing Guidelines

1. Target differential impedance of 100 ohms, +/-10%.
2. Traces should be as short and symmetrical as possible.
3. The differential traces should be length-matched to within 0.005" within pairs.
4. Maximum of 4-inch trace lengths for differential pairs.
5. Differential pair should be routed adjacent to a GND plane.
6. AC coupling capacitors should be placed close to PCI Express transmitter.

For additional information, please refer to the PCI Express® Card Electromechanical Specification Revision 1.1, available from PCI-SIG: www.pcisig.com

3 Flash Interface Considerations

The 9725 requires a 8MB serial flash to store the firmware image. The flash sector size must not be larger than 64kB.

The following table lists suitable Flash memory devices for use with the 9725, though other devices may be supported. Please contact Hifn for further information regarding compatible devices.

Table 3-1. Supported Flash Memory Devices

Manufacturer	Part Number	Size (Bytes)
Numonyx	M25P64VMF6TP	8MBytes
	M25P64VMF6P	8MBytes
Spansion	S25FL064A0LMFI003	8MBytes

There are no special trace length requirements for the Flash interface.

4 Termination Requirements

4.1 PULLUP, PULLDN, NC Pins

All pins labeled PULLUP must be connected to a 1K ohm pull-up resistor to VDD33. All pins labeled PULLDN must be connected to a 10K ohm pull-down resistor to ground.

All pins labeled NC must be left unconnected.

Although optional, the JTAG_TRST_N signal must be pulled low for normal board operation.

4.2 DMA_PLL_REF_CLK Pin

The DMA_PLL_REF_CLK input pin can be driven either from a crystal oscillator or from a PLL clock generator. The clock source should be placed as close as possible to the 9725. See the *9725 Data Sheet*, DS-0161, for the detailed clock requirements.

A crystal oscillator, if used, must be a 3.3V device with a stability of +/- 150 ppm or better. A suitable crystal oscillator is the Pericom S1613B-25.0000 device. A 33-ohm series termination resistor should be placed near the oscillator output pin.

A PLL clock generator, if used, must have 400ps or less of jitter.

5 Thermal Requirements

This chapter describes the heatsink and optional thermal monitoring device requirements.

5.1 Heatsink

All customer designs will require unique system thermal analysis to determine if a heat sink is required, and if so, the required characteristics of that heatsink. Please refer to the *9725 Data Sheet*, DS-0161, for the detailed 9725 thermal specifications.

Hifn used a heatsink on the 9725 evaluation card from Radian Heatsinks, part #HIF008C (www.radianheatsinks.com), and shown in Figure 5-1 below. This heatsink was designed for an ambient temperature of 55C and 0 LFM airflow.

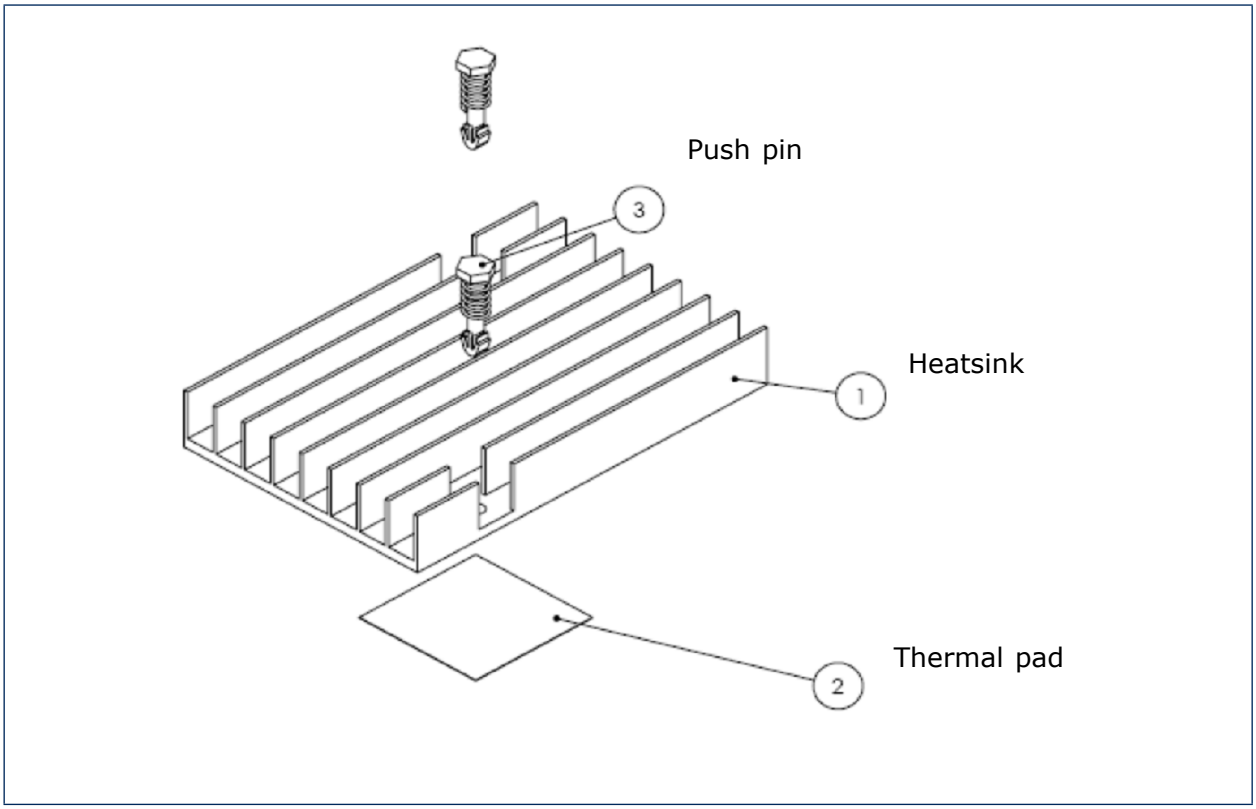

Figure 5-1. Example Heatsink

5.2 Thermal Monitoring Device

The 9725 contains an internal PN junction which may be optionally used to monitor the 9725 junction temperature. A 9725 design that employs this feature will require an additional thermal monitoring device.

As shown in Figure 5-2, the MAX6681MEE provides an example of a dual-channel digital thermometer thermal device that accurately measures the temperature of its own die and one remote PN junction. The MAX6681MEE includes pin-programmable default temperature thresholds to report an over-temperature alarm. The over temperature thresholds are both hardware and software programmable. The over temperature thresholds may be set in hardware by strapping pins CRIT0 and CRIT1. For detailed information, please refer to the 9725 Evaluation Card schematics and the MAX6681MEE Data Sheet.

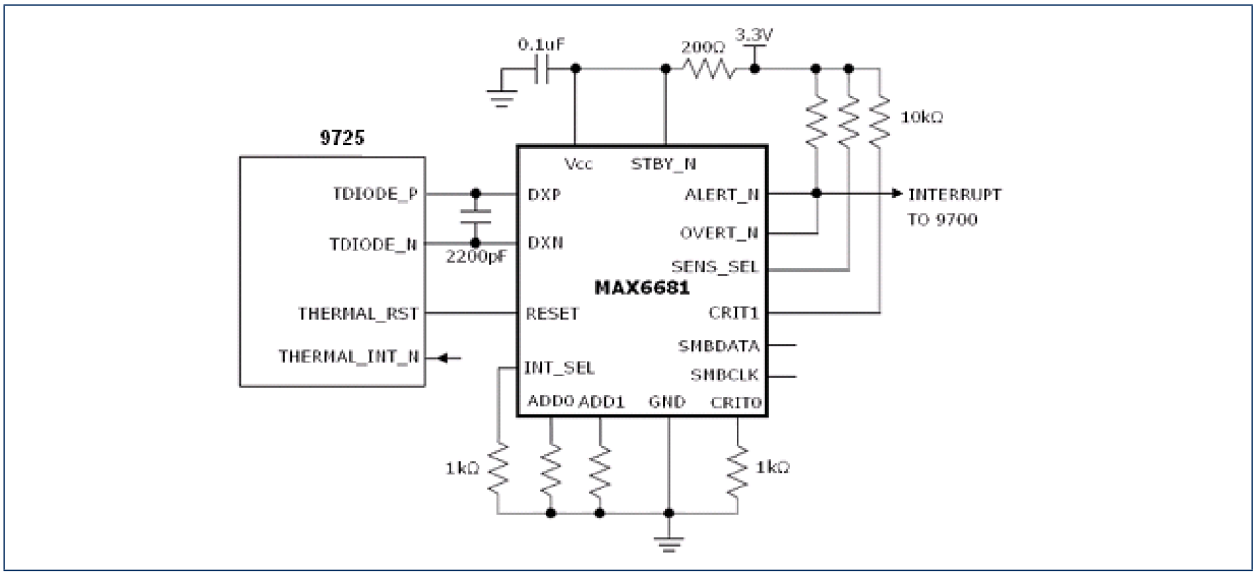

Figure 5-2. Example Thermal Monitoring Device

If the thermal chip is not used, the 9725 THERMAL_INT_N pin should be pulled up to 3.3V with a 10K ohm resistor.

I Document Revisions

Documentation Revisions include additions, deletions, and modifications made to this document. This section identifies the changes made for each release of the document.

I.1 Document Revision A

Initial release.

I.2 Document Revision 00

Update 1. Changed part number from 9700 to 9725 throughout.

Update 2. Removed preliminary marking for production release.

Update 3. Section 1.2 Digital and Analog Power Supplies: removed this section as it is redundant with the data sheet.

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